HOLT INTEGRATED CIRCUITS INC.

May 2022

HI-25850

MIL-STD-1553 / 1760 3.3V Dual Transceiver with Integrated Transformers Featuring 1.8V and 2.5V Compatible Digital I/O and Tail-Off Control

DESCRIPTION

The HI-25850 is an ultra-low power CMOS dual transceiver with integrated transformers designed to meet the requirements of the MIL-STD-1553 and MIL-STD-1760 specifications. The dual transceivers with integrated transformers provide a single part solution for interfacing a protocol IC or FPGA to a dual redundant MIL-STD-1553 bus.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the integrated isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter. The receiver section of the each bus converts the 1553 bus differential data to complementary CMOS / TTL data suitable for inputting to a Manchester decoder. Each bus has its own Receive Enable input, which forces both receive output signals to the bus idle state (logic "0") when disabled.

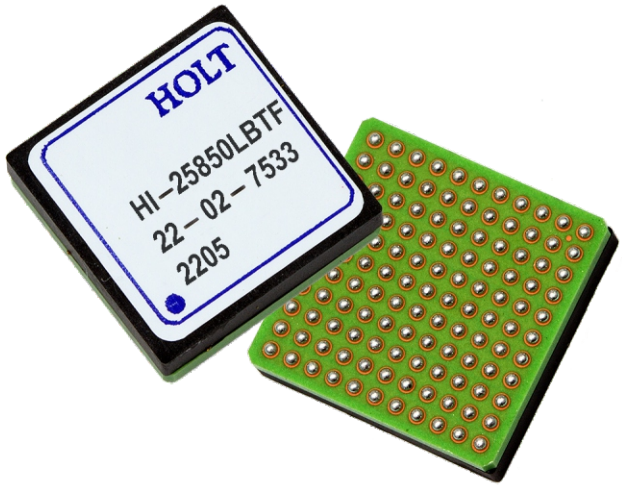
The device also features 1.8V, 2.5V and 3.3V compatible digital I/O, making it easier to interface with a broad range of FPGAs.

To reduce end-of-transmission residual voltage offset (”tail-off”), logic-level transmit signal inputs can be clocked-in to synchronize their rise/fall transitions. This compensates for timing mismatch or transmit signal path propagation differences caused by board layout. When sub-optimal board design consistently presents tail-off magnitudes close to or exceeding mandatory limits, another unique option lets the user select a bus-specific level of digital tail-off compensation.

The HI-25850 also provides optional Receive output pulse extension. With traditional MIL-STD-1553 transceivers, low amplitude receive signals can result in RX/nRX pulses less than 100ns wide. When this feature is enabled, RX/nRX output pulse widths do not drop below 180ns, greatly simplifying decoder design and enhancing noise performance.

APPLICATIONS

- MIL-STD-1553 Terminals
- Flight Control and Monitoring
- Radar Systems
- ECCM Interfaces and Stores Management
- Test Equipment
- Sensor Interfaces and Instrumentation



FEATURES

- Compliant to MIL-STD-1553A and B, MIL-STD-1760 and ARINC 708A
- Integrated MIL-STD-1553 transformers
- 3.3V single supply operation
- Input data synchronization.
- Tail-off compensation control.
- Receiver output pulse-width extension control.

SIGNAL DESCRIPTIONS

PIN	FUNCTION	DESCRIPTION	
GND	power supply	Ground	
VDDB	power supply	+3.3 volt power for transceiver B	
TXB	digital input	Transmitter B digital data input, non-inverted	Internal pull-down resistor
$\overline{\text{TXB}}$	digital input	Transmitter B digital data input, inverted	Internal pull-down resistor
TXINHB	digital input	Transmit inhibit, bus B. If high BUSB, $\overline{\text{BUSB}}$ disabled	Internal pull-down resistor
RXENB	digital input	Receiver B enable. If low, forces RXB and $\overline{\text{RXB}}$ low	Internal pull-up resistor
RXB	digital output	Receiver B output, non-inverted	
$\overline{\text{RXB}}$	digital output	Receiver B output, inverted	
ENPEXTB	digital input	Enable pulse extension for receiver B	Internal pull-up resistor
BUSB	analog	MIL-STD-1553 Bus B driver, positive signal	
$\overline{\text{BUSB}}$	analog	MIL-STD-1553 Bus B driver, negative signal	
VDDIO	power supply	Power for digital I/O. Supports 1.8V, 2.5V or 3.3V.	
ENCLKB	digital input	Enable input synchronization for transmitter B	Internal pull-down resistor
CLKB	digital input	Synchronization clock input for transmitter B	Internal pull-down resistor
TOC1B	digital input	Tail-off adjust transmitter B. (See Table 2)	Internal pull-down resistor
TOC0B	digital input	Tail-off adjust transmitter B. (See Table 2)	Internal pull-down resistor
TOC0A	digital input	Tail-off adjust transmitter A. (See Table 2)	Internal pull-down resistor
TOC1A	digital input	Tail-off adjust transmitter A. (See Table 2)	Internal pull-down resistor
CLKA	digital input	Synchronization clock input for transmitter A	Internal pull-down resistor
ENCLKA	digital input	Enable input synchronization for transmitter A	Internal pull-down resistor
$\overline{\text{BUSA}}$	analog	MIL-STD-1553 Bus A driver, negative signal	
BUSA	analog	MIL-STD-1553 Bus A driver, positive signal	
VDDA	power supply	+3.3 volt power for transceiver A	
ENPEXTA	digital input	Enable pulse extension for receiver A	Internal pull-up resistor
$\overline{\text{RXA}}$	digital output	Receiver A output, inverted	
RXA	digital output	Receiver A output, non-inverted	
RXENA	digital input	Receiver A enable. If low, forces RXA and $\overline{\text{RXA}}$ low	Internal pull-up resistor
TXINHA	digital input	Transmit inhibit, bus A. If high BUSA, $\overline{\text{BUSA}}$ disabled	Internal pull-down resistor
TXA	digital input	Transmitter A digital data input, non-inverted	Internal pull-down resistor
$\overline{\text{TXA}}$	digital input	Transmitter A digital data input, inverted	Internal pull-down resistor
TOC2A	digital input	Tail-off adjust transmitter A. (See Table 2)	Internal pull-down resistor
TOC2B	digital input	Tail-off adjust transmitter B. (See Table 2)	Internal pull-down resistor
BUSATC	analog input	BUS A transformer primary connection, positive signal. MUST be connected to TXOUTA on PWB.	
$\overline{\text{BUSATC}}$	analog input	BUS A transformer primary connection, negative signal. MUST be connected to $\overline{\text{TXOUTA}}$ on PWB.	
BUSBTC	analog input	BUS B transformer primary connection, positive signal. MUST be connected to TXOUTB on PWB.	
$\overline{\text{BUSBTC}}$	analog input	BUS B transformer primary connection, negative signal. MUST be connected to $\overline{\text{TXOUTB}}$ on PWB.	
TXOUTA	analog output	BUS A transceiver output, positive signal. MUST be connected to BUSATC on PWB.	
$\overline{\text{TXOUTA}}$	analog output	BUS A transceiver output, negative signal. MUST be connected to $\overline{\text{BUSATC}}$ on PWB.	
TXOUTB	analog output	BUS B transceiver output, positive signal. MUST be connected to BUSBTC on PWB.	
$\overline{\text{TXOUTB}}$	analog output	BUS B transceiver output, negative signal. MUST be connected to $\overline{\text{BUSBTC}}$ on PWB.	

Table 1. Signal Descriptions

BALL DIAGRAM

Top View

	11	10	9	8	7	6	5	4	3	2	1	
L	VDDIO	nBUSB TC	DNC	DNC	TX INHB	TXB	DNC	DNC	DNC	DNC	DNC	L
K	VDDIO	DNC	DNC	ENP EXTB	nRXB	RXB	DNC	DNC	DNC	DNC	BUSB	K
J	EN CLKB	DNC	DNC	VDD	GND	RXENB	DNC	TOC2B	DNC	DNC	BUSB	J
H	DNC	BUSB TC	DNC	DNC	GND	nTXB	DNC	DNC	DNC	DNC	nBUSB	H
G	TOC1A	CLKB	TOC1B	VDD	GND	VDD	GND	VDD	DNC	nTX OUTB	nBUSB	G
F	CLKA	TOC0B	TOC0A	GND	VDD	GND	VDD	GND	VDD	nTX OUTA	TX OUTB	F
E	VDDIO	EN CLKA	DNC	VDD	GND	VDD	GND	VDD	DNC	TX OUTA	BUSA	E
D	DNC	VDDIO	nBUSA TC	RXA	VDD	DNC	DNC	DNC	TOC2A	DNC	BUSA	D
C	BUSA TC	DNC	DNC	GND	RXENA	VDD	DNC	DNC	DNC	DNC	nBUSA	C
B	DNC	DNC	DNC	GND	TXA	TX INHA	GND	DNC	DNC	DNC	nBUSA	B
A	DNC	VDD	ENP EXTA	nRXA	nTXA	GND	DNC	DNC	DNC	DNC	DNC	A
	11	10	9	8	7	6	5	4	3	2	1	

Notes:

a. DNC: Do Not Connect.
b. All balls denoted VDD **must** be connected to 3.3V DC power.
c. All balls denoted GND **must** be connected to circuit ground.
d. Prefix “n” denotes a negative (inverted) signal e.g. nBUSA = $\overline{\text{BUSA}}$, etc.
e. Ball L10 **must** be connected to ball G2 externally on PWB. Ball H10 **must** be connected to ball F1 externally on PWB.
f. Ball C11 **must** be connected to ball E2 externally on PWB. Ball D9 **must** be connected to ball F2 externally on PWB.

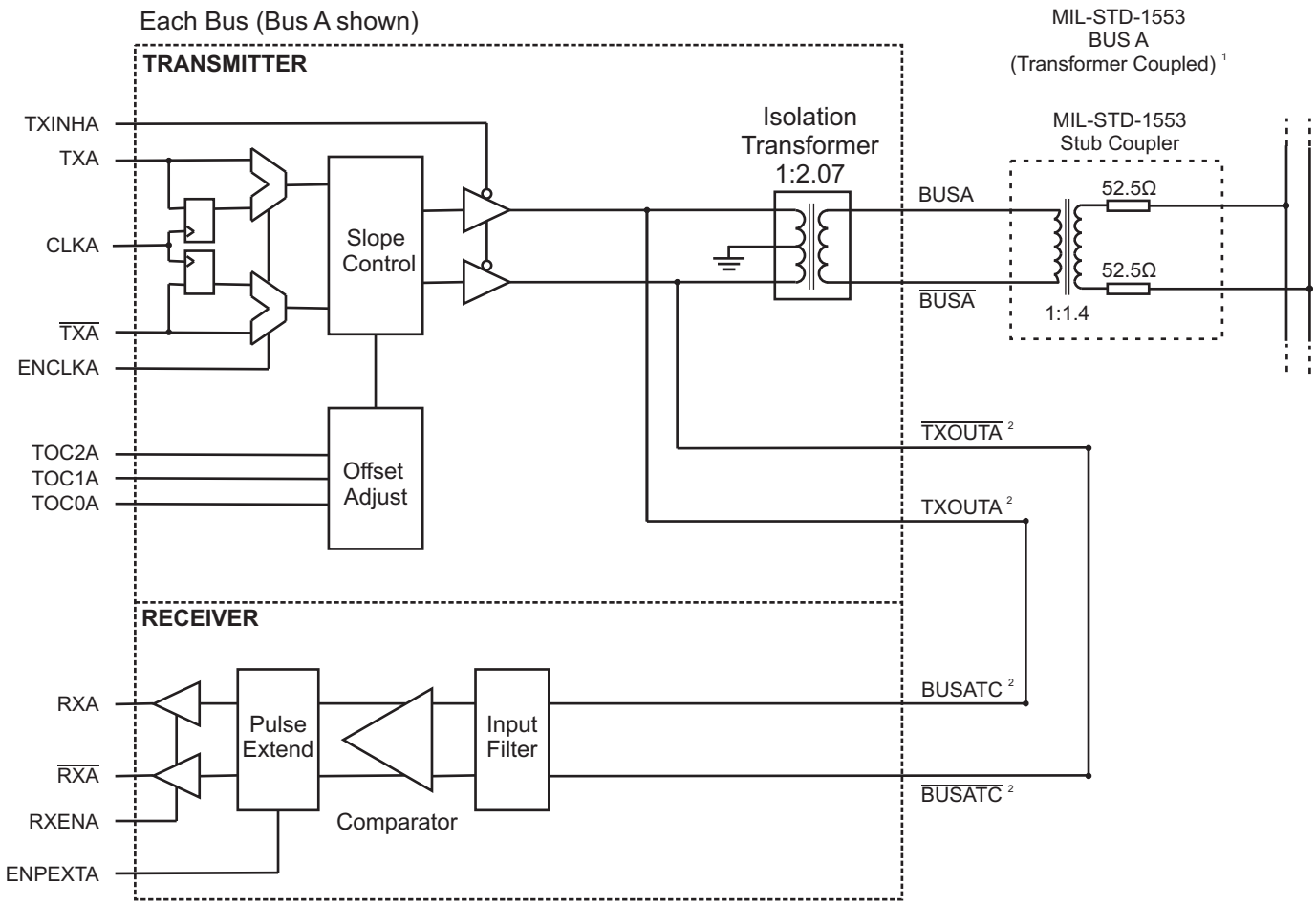


Figure 1. Block Diagram

NOTE 1: Transformer Coupled option shown.
For Direct Coupled option (1:2.65 transformer ratio), please contact Holt.

NOTE 2: BUSATC and TXOUTA **must** be shorted on PWB board. Not connected internally.
BUSATC and TXOUTA **must** be shorted on PWB board. Not connected internally.
BUSBTC and TXOUTB **must** be shorted on PWB board. Not connected internally.
BUSBTC and TXOUTB **must** be shorted on PWB board. Not connected internally.
See also package 121BGA3 drawing

FUNCTIONAL DESCRIPTION

The HI-25850 dual MIL-STD-1553 bus transceiver contains a differential voltage source driver, a differential analog bus receiver and integrated transformers for each bus. It is designed for applications using a MIL-STD-1553B communications bus.

TRANSMITTER

For each bus, data input to the HI-25850 transmitter is a pair of complementary CMOS inputs TXA and $\overline{\text{TXA}}$ for Bus A, with a corresponding signal pair for Bus B. The transmitter accepts Manchester II bi-phase data and converts it to differential analog voltages on BUSA and $\overline{\text{BUSA}}$, or BUSB and $\overline{\text{BUSB}}$. The transceiver outputs are transformer-coupled to the MIL-STD-1553 data bus. This produces a nominal voltage on the bus of 7.5 Volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when TXA and $\overline{\text{TXA}}$ (or TXB and $\overline{\text{TXB}}$) are both driven to the same logic state. A bus transmitter is also forced to the high impedance state when logic “1” is applied at the TXINHA (or TXINHB) transmit inhibit input, regardless of the TXA and $\overline{\text{TXA}}$ (or TXB and $\overline{\text{TXB}}$) input condition.

TRANSMIT-INDUCED TAIL-OFF (OFFSET)

A prevalent concern when designing MIL-STD-1553 terminals goes by a number of names, including transmit "output symmetry", "tail-off" and "offset". This is a transmit-induced phenomenon that occurs on the bus following long transmissions, when one or more design or operating factors are less than ideal. Slight imbalances in the transmitted analog signal voltage cause accumulation of energy in the terminal's isolation transformer. When transmission ends and the transceiver bus interface goes to the Standby or receive mode, a temporary DC voltage is expressed on the bus. This "tail-off" voltage can have positive or negative polarity; it decays exponentially, often persisting for 10 to 20µs depending on magnitude. See Figure 2. Good positive/negative signal matching (or short message transmissions) result in low tail-off magnitude, while serious mismatch problems combined with long transmissions can cause the DC stub voltage to approach or exceed 0.25 V peak-peak.

Design and product use factors that influence tail-off include:

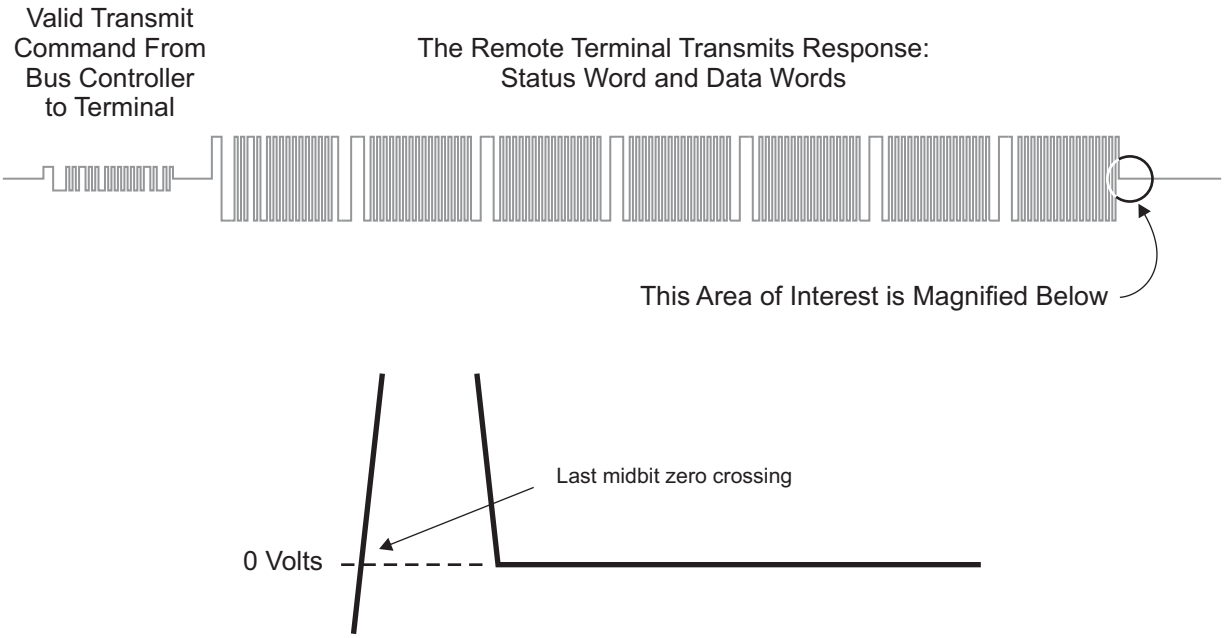
- the data patterns being transmitted. Some repeating data word values cause greater tail-off magnitude than random data or other repeating data patterns. For Holt transceivers, 32-word transmissions using repeating 0x0000 data usually give worst case tail-off magnitude
- timing skew for TX and $\overline{\text{TX}}$ input signals generated by the encoder
- mismatched conductor length or impedance between encoder and transceiver drive signal inputs for TX and $\overline{\text{TX}}$
- mismatched positive/negative drive voltage in the transceiver
- mismatched positive/negative rise and fall times in the transceiver
- poor signal path impedance matching between transceiver positive/negative drive output pins and the isolation transformer
- imbalance between positive/negative half-windings in the center-tapped isolation transformer.

Holt carefully designs its MIL-STD-1553 transceivers for symmetry and matched positive/negative drive characteristics to minimize transceiver contribution to tail-off. We strongly urge designers to prioritize system topology and layout so that MIL-STD-1553 bus interface characteristics are considered first. All too often, it seems like 1553 bus interface is a late consideration, resulting in marginal performance (or worse) and considerable time wasted on redesign.

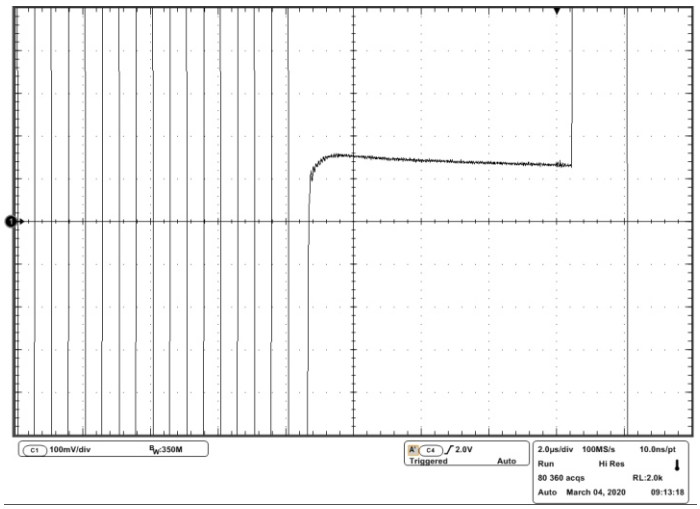
The Manchester II encoder (often implemented in FPGA or CPLD) should be close to the transceiver and uses Hardware Description Language (HDL) that carefully matches positive/negative time intervals and uses synchronous switching.

A design may deviate from ideal characteristics when circumstances prevail. Mismatch caused by layout deficiency often results in a consistent tail-off range for each bus, with message-to-message tail-off magnitude changes caused by message length and data differences. Bus A tail-off rarely matches Bus B. Sometimes the contribution from various factors cancels out, moving the tail-off voltage range for that bus closer to zero. Sometimes the various contributions conspire to raise average tail-off magnitude away from zero. Until now, designers had few options other than redesign when unacceptable tail-off occurred. The HI-25850 offers two optional provisions to minimize systemic tail-off occurrence, namely Input Data Synchronization and Bus Tail-off Adjustment. These are both described in the following sections.

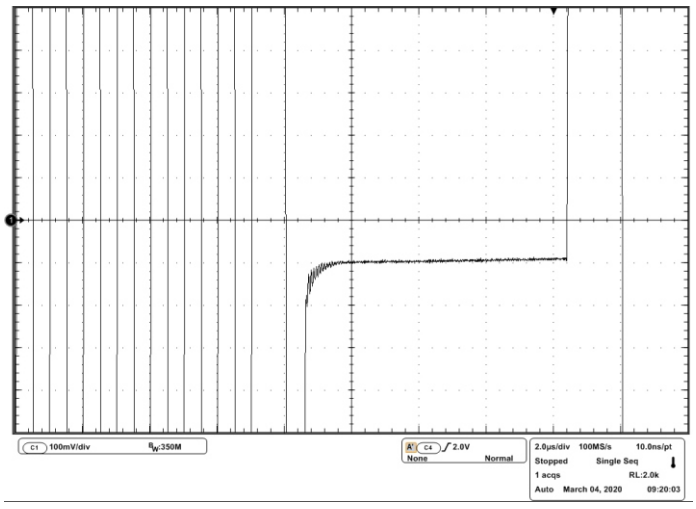
FUNCTIONAL DESCRIPTION (cont.)



a) Ideal Waveform Has No Tail-off or Ringing



b) Exponentially-Decaying Positive Tail-off



c) Exponentially-Decaying Negative Tail-off

Figure 2. Transmit-induced Tail-off (Offset)

FUNCTIONAL DESCRIPTION (cont.)

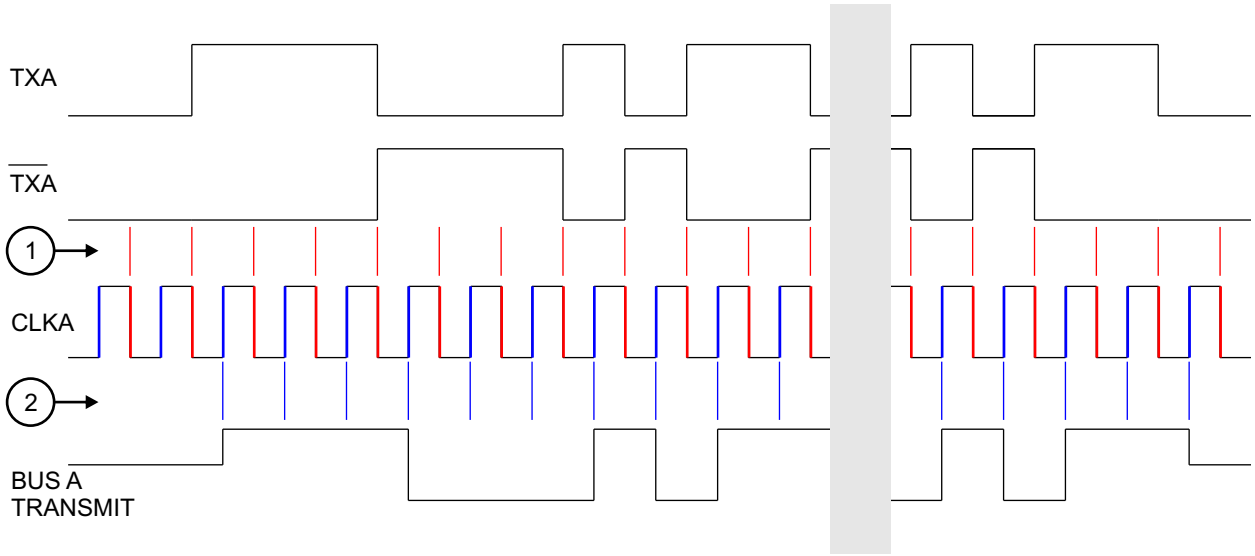
INPUT DATA SYNCHRONIZATION

Timing skew between TX and $\overline{TX}$ is a common cause of MIL-STD-1553 end-of-message tail-off (output symmetry). To align input signal edges, the HI-25850 offers optional TX and $\overline{TX}$ input synchronization.

Using Bus A as an example …

- When input pin ENCLKA is logic-1, rising edge-triggered flip-flops synchronize the logic-level TXA and $\overline{TXA}$ transmit inputs. This minimizes timing error and resultant tail-off (output symmetry) distortion.
- Refer to Figures 2 and 3. If not clocked continuously between bus transmissions, the idle state for transceiver input CLKA is high. To transmit on the 1553 bus, the host FPGA launches Manchester-encoded TXA/$\overline{TXA}$ data on each falling edge of CLKA and the HI-25850 latches the incoming TXA/$\overline{TXA}$ transmit data on the CLKA rising edge. Setup and hold times for the TXA/$\overline{TXA}$ signals are 10ns each, relative to CLKA rising edge. For Figure 3 example, the CLKA frequency is 2.0 MHz, generated by the encoding FPGA.
- When ENCLKA = 0, the HI-25850 TXA and $\overline{TXA}$ clocked input flip-flops are bypassed; the CLKA pin is ignored. The BUSA and $\overline{BUSA}$ output signals directly follow the TXA and $\overline{TXA}$ inputs.

Bus B synchronization uses a duplicate set of input pins (ENCLKB, CLKB, TXB and $\overline{TXB}$) to control BUSB and $\overline{BUSB}$.



In this example, CLKA = 2.0 MHz and TX data refreshes every 500 ns.
1. TX data from FPGA should update on CLKA falling edge.
2. TX data is clocked into HI-25850 on CLKA rising edge.
3. Propagation delay to bus output not shown.

Figure 3. Transmit Signal Input Synchronization Option

FUNCTIONAL DESCRIPTION (cont.)

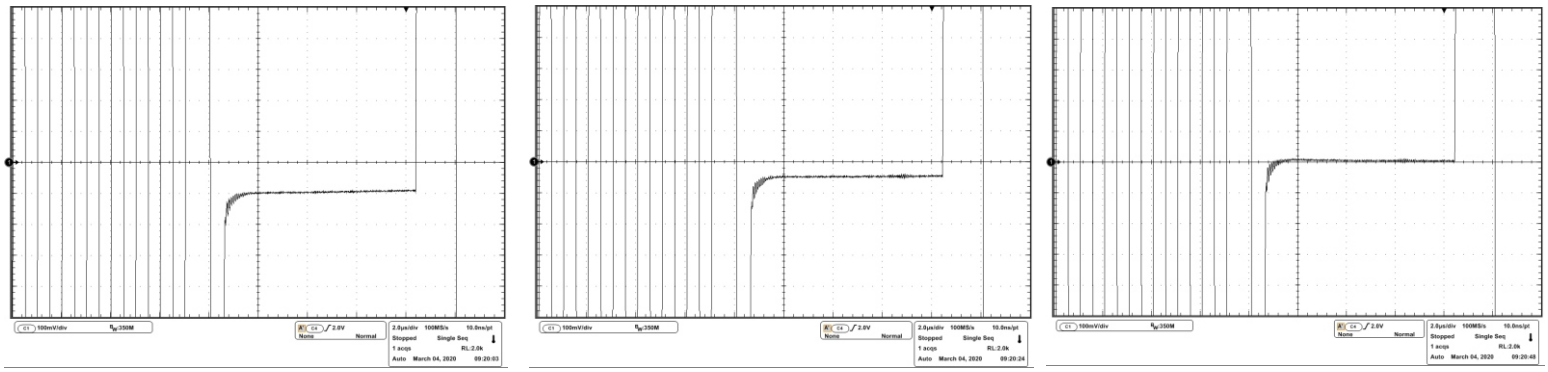
BUS TAIL-OFF ADJUSTMENT

A second provision affecting tail-off performance is output trimming. This method compensates drive characteristics when the HI-25850 drives mismatched signal path impedance between the positive/negative drive output pins and the isolation transformer. Bus A and Bus B each have 3 input pins, TOC[2:0], which present a 3-bit binary argument. Two of the 8 possible states provide zero compensation, and pull-downs force the 3 pins to 0-0-0, a zero compensation state if the TOC pins are left open. Three states provide small-medium-large compensation levels for positive-going tail-off while the three remaining states do the same for negative-going tail-off. Table 2 lists the TOC[2:0] codes and their nominal effect on offset for a transformer-coupled configuration. Figures 4 and 5 illustrate the effect of positive and negative compensation on tail-off. It is envisioned that this would be a one-time setup to compensate for board layout deficiencies that cause consistent tail-off trouble in the same direction. The circuit applies incredibly slight changes to transmitted signal rise time and fall time to achieve compensation. Very slight differences (<1ns) applied to all state changes in a long message have a surprising effect on tail-off level.

NOTE: The compensation values listed below are average values using 32-word messages measured across 6 data patterns (0x0000, 0xFFFF, 0x5555, 0xAAAA, 0x7FFF and 0x8000) in a laboratory test set-up. The applied tail-off shift is proportional to message length. It is recommended that the user evaluate each individual application before applying tail-off compensation.

TOC2	TOC1	TOC0	Tail-off / Offset Shift
0	0	0	0 mV (No correction)
0	0	1	+ 50 mV shift
0	1	0	+ 100 mV shift (for negative tail-off)
0	1	1	+ 150 mV shift
1	0	0	0 mV (No correction)
1	0	1	- 50 mV shift
1	1	0	- 100 mV shift (for positive tail-off)
1	1	1	- 150 mV shift

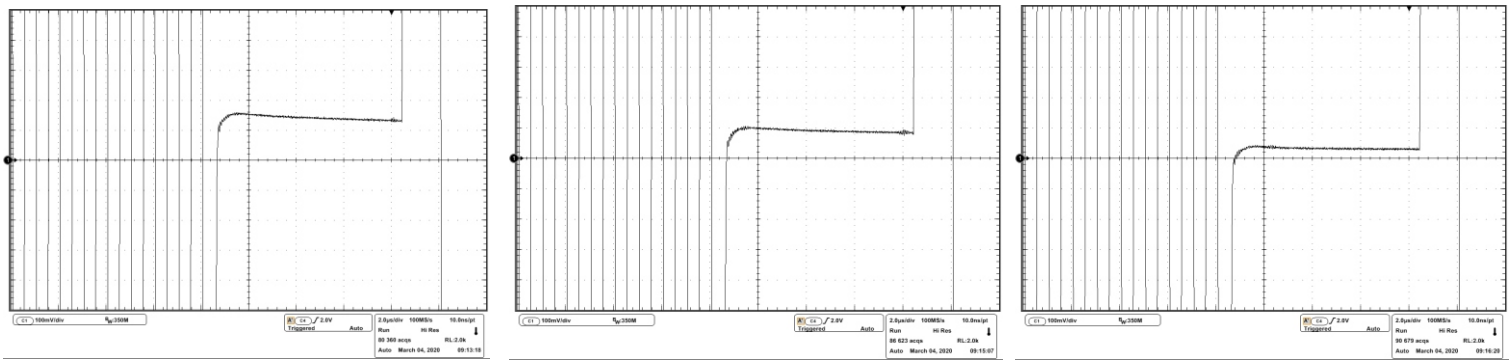
Table 2. TOC[2:0] codes



a) Uncompensated, TOC[2:0] = 000 or 100 b) TOC[2:0] = 001 c) TOC[2:0] = 010

Figure 4. Effect of Positive Compensation on Negative Tail-off (Offset)

FUNCTIONAL DESCRIPTION (cont.)



a) Uncompensated, TOC[2:0] = 000 or 100 b) TOC[2:0] = 101 c) TOC[2:0] = 110

Figure 5. Effect of Negative Compensation on Positive Tail-off (Offset)

RECEIVER

The receiver accepts bi-phase differential analog signals from the MIL-STD-1553 bus through the same transformer-coupled interface . The receiver differential input stage drives a filter and threshold comparator to produce CMOS data at the RXA and $\overline{\text{RXA}}$ (or RXB and $\overline{\text{RXB}}$) output pins. When the MIL-STD-1553 bus is idle and RXENA (or RXENB) receiver enable inputs are high, the corresponding RX and $\overline{\text{RX}}$ output pins will be logic “0”.

Both receiver outputs are forced to the bus idle state (logic “0”) when RXENA or RXENB is low.

RECEIVER OUTPUT PULSE EXTENSION

A unique feature of the HI-25850 is RX and $\overline{\text{RX}}$ output pulse extension. When receiving differential signals near the MIL-STD-1553 minimum amplitude specification (860 mVpp when transformer-coupled), traditional transceivers produce narrow output pulses at RX and $\overline{\text{RX}}$, because the time that analog bus voltage exceeds the receiver threshold is much shorter than for a nominal or large amplitude bus voltage. The HI-25850 receiver pulse outputs can optionally be stretched so that any comparator pulse outputs from RX and $\overline{\text{RX}}$ have a minimum pulse width of 180ns. This function is enabled by strapping the ENPEXT configuration pin high. When ENPEXT is low, the part reverts to traditional operation where RX and $\overline{\text{RX}}$ output pulses reflect just the time that analog bus voltage exceeds comparator threshold voltage.

Warning: Utilizing the receiver output pulse extension feature will improve receiver sensitivity, which degrades noise immunity. Therefore, careful consideration should be given to enabling this feature in applications required to pass RT validation noise rejection test.

MIL-STD-1553 BUS INTERFACE

In a transformer-coupled interface (see Figure 1), the transceiver is connected to a 1:2.07 turns-ratio isolation transformer which is connected to the main bus using a 1:1.4 turns-ratio coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus. The coupling transformer and coupling resistors are commonly integrated in a single device known as a stub coupler.

Figure 7 shows a test circuit for measuring electrical characteristics of transformer-coupled interfaces respectively. (See electrical characteristics on the following pages).

POWER SUPPLY SEQUENCING

The power supply sequencing of VDDA/VDDB versus VDDIO should be controlled to prevent large currents during turn-on and turn-off. The recommended sequence is VDDA/VDDB followed by VDDIO, always ensuring that VDDA/VDDB is the most positive supply within 1ms.

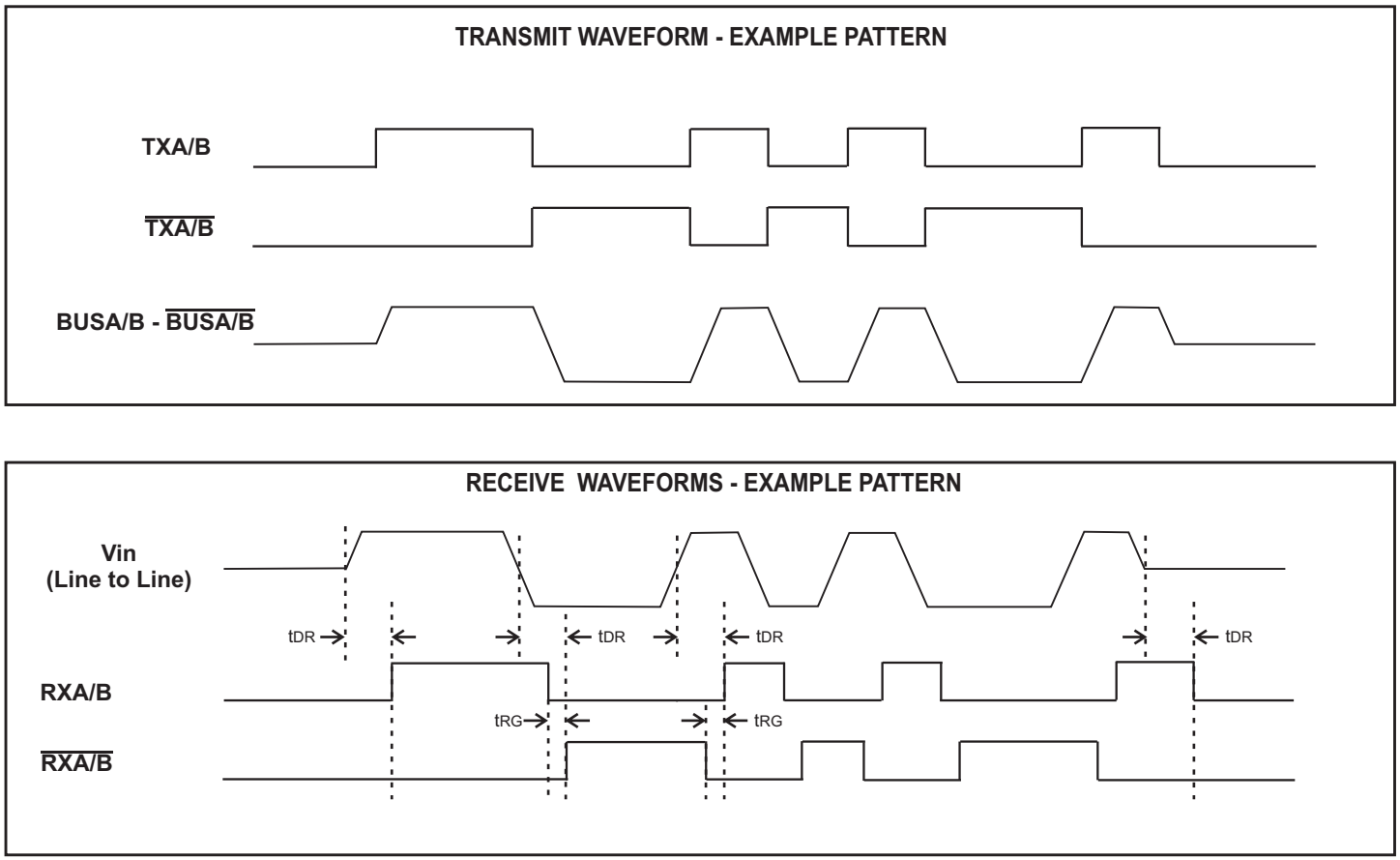


Figure 6. Transmit and Receive Waveform Examples

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.3 V to +5 V
Logic input voltage range	-0.3 V dc to +3.6 V
Voltage at BUSA/B or $\overline{BUSA/B}$ pins	+/-7 V
Receiver differential voltage	50 Vp-p
Reflow Solder Temperature	245°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages

V_{DD} ..... 3.3V... ±5%

Temperature Range

Industrial ..... -40°C to +85°C
Hi-Temp ..... -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.14 V to 3.46V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Transceiver Supply Voltage	V_{DD}		3.14	3.30	3.46	V
Total Supply Current	I_{CC1}	Not Transmitting		30	35	mA
	I_{CC2}	Transmit one bus @ 50% duty cycle, 78.8Ω resistive load		310	330	mA
	I_{CC3}	Transmit one bus @ 100% duty cycle, 78.8Ω resistive load		630	670	mA
Power Dissipation See Note 1 on next page	PD_1	Not Transmitting		0.1	0.12	W
	PD_2	Transmit one bus @ 100% duty cycle, 78.8Ω resistive load		0.89	1.0	W
Digital I/O Supply Voltage	V_{DDIO}	1.8V Digital I/O	1.65	1.8	1.95	V
		2.5V Digital I/O	2.3	2.5	2.7	V
		3.3V Digital I/O	3.0	3.3	3.6	V
Digital I/O Supply Current	I_{VDDIO}				15	mA
Min. Input Voltage (High)	V_{IH}	Digital inputs, V_{DDIO} = V_{DD} = 3.3V	70%			VDD
Max. Input Voltage (Low)	V_{IL}	Digital inputs, V_{DDIO} = V_{DD} = 3.3V			30%	VDD
Min. Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs V_{DDIO} = V_{DD} = 3.3V	90%			VDD
Max. Output Voltage (Low)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs V_{DDIO} = V_{DD} = 3.3V			10%	VDD
Min. Input Voltage (High)	V_{IH}	Digital inputs, V_{DDIO} = 2.5V, V_{DD} = 3.3V	1.7			V
Max. Input Voltage (Low)	V_{IL}	Digital inputs, V_{DDIO} = 2.5V, V_{DD} = 3.3V			0.7	V
Min. Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs V_{DDIO} = 2.5V, V_{DD} = 3.3V	2.3			V
Max. Output Voltage (Low)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs V_{DDIO} = 2.5V, V_{DD} = 3.3V			0.2	V

DC ELECTRICAL CHARACTERISTICS (cont.)

V_{DD} = 3.14 V to 3.46V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Min. Input Voltage (High)	V_{IH}	Digital inputs, V_{DDIO} = 1.8V, V_{DD} = 3.3V	1.17			V
Max. Input Voltage (Low)	V_{IL}	Digital inputs, V_{DDIO} = 1.8V, V_{DD} = 3.3V			0.63	V
Min. Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs V_{DDIO} = 1.8V, V_{DD} = 3.3V	1.35			V
Max. Output Voltage (Low)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs V_{DDIO} = 1.8V, V_{DD} = 3.3V			0.45	V
Input Current (High)	I_{IH}	RXEN, ENPEXT, ENCLK	-50		20	µA
Pull-Down Current (High)	I_{IHP}	TX, $\overline{TX}$, TXINH, TOC, CLK	10	20	50	µA
Input Current (Low)	I_{IL}	TX, $\overline{TX}$, TXINH, ENCLK, TOC, CLK	-20			µA
Pull-Up Current (Low)	I_{ILP}	RXEN, ENPEXT	-50	-20	-10	µA
RECEIVER						
Input resistance	R_{IN}	Differential (at chip pins)	5			kOhm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input common mode voltage	V_{ICM}		-10.0		10.0	V-pk
Theshold Voltage - Transformer-coupled Detect	V_{THD}	1 MHz Sine Wave Measured at Point "A_T" in Figure 7 RXA/B, $\overline{RXA/B}$ pulse width >70 ns	0.86			Vp-p
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.20	Vp-p
TRANSMITTER						
Output Voltage Transformer coupled	V_{OUT}	70 ohm load (Measured at Point "A_T" in Figure 7)	20.0		27.0	Vp-p
Output Noise	V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage Transformer coupled	V_{DYN}	70 ohm load (Measured at Point "A_T" in Figure 7)	-250		250	mV
Output Capacitance	C_{OUT}	1 MHz sine wave			15	pF

Note 1: While one bus continuously transmits, the power delivered by the 3.3V power supply is 3.3V × 630mA typical = 2.1W. Of this, 0.89W is dissipated in the device, the remainder (1.2W) in the load.

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.14 V to 3.46 V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "AT" in Figure 7 unless otherwise specified)						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$			450	ns
Receiver gap time ENPEXT = 0	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses. 1 MHz sine wave applied at point "AT" Figure 7, amplitude range 0.86 Vp-p to 27.0Vp-p	70		365	ns
Receiver gap time ENPEXT = 1	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses. 1 MHz sine wave applied at point "AT" Figure 7, amplitude range 0.86 Vp-p to 27.0Vp-p	180		200	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "AT" in Figure 7)						
Driver Delay	t_{DT}	TXA/B, $\overline{TXA/B}$ to BUSA/B, $\overline{BUSA/B}$			160	ns
Rise time	tr	70 ohm load	100	150	300	ns
Fall Time	tf	70 ohm load	100	150	300	ns
Inhibit Delay	t_{DI-H}	Inhibited output			100	ns
	t_{DI-L}	Active output			150	ns
Tx/$\overline{Tx}$ data set-up time to CLK rising edge	t_{Tx-S}	ENCLK pin enabled (high)	10			ns
Tx/$\overline{Tx}$ data hold time after CLK rising edge	t_{Tx-H}	ENCLK pin enabled (high)	10			ns

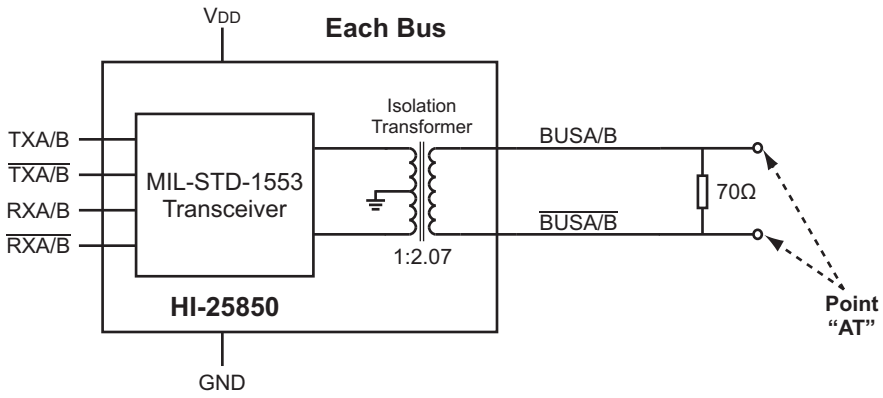


Figure 7. Transformer Coupled Test Circuit

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt's family of MIL-STD-1553 transceivers. Layout considerations, as well as recommended interface and protection components are included.

ORDERING INFORMATION

HI - 25850 LB x x

PART NUMBER	BALL FINISH
Blank	Leaded Balls (Sn63Pb37)
F	Pb-free, RoHS compliant, SAC305 Solder Balls (Sn96.5/Ag3/Cu0.5)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
LB	121 BALL GRID ARRAY - BGA (121BGA3)

*** NOTE:** All part variants above use a Transformer Coupled bus interface.
For Direct Coupled option (1:2.65 transformer ratio), please contact Holt.

REVISION HISTORY

Document	Rev.	Date	Description of Change
DS25850	New	06/15/2020	Initial Release.
	A	08/14/2020	Clarify description of BUSATC, $\overline{\text{BUSATC}}$, BUSBTC and $\overline{\text{BUSBTC}}$ signals.
	B	09/10/2020	Update tail-off compensation values in Table 2 and example plots to match HI-15850. Change package designation of BGA drawing from BGA3 to BGA4.
	C	04/19/2021	Change part number from HI-25850LBx to HI-25850PBx. There is no change in the device itself, only in nomenclature.
	D	02/22/2022	Replace HI-25850PBx device with HI-25850LBx. Replace 121BGA4 package drawing with 121BGA3 package drawing.
	E	02/25/2022	Correct typo in Table 1, Signal Descriptions. BUSATC, $\overline{\text{BUSATC}}$, BUSBTC and $\overline{\text{BUSBTC}}$ should all be Analog Inputs, not Outputs.
	F	03/09/2022	Correct typo in Ball Diagram. Ball K8 should be labeled ENPEXTB, not ENPEXTA.
	G	04/18/2022	Update supply current and power dissipation numbers in DC Electrical Characteristics. Add note on Power Supply Sequencing.
	H	05/27/2022	Add note regarding use of receiver output pulse extension feature.

Ball Grid Array

inches (millimeters)
Package Type: 121BGA3